2.25W Stereo Audio Power Amplifier

DESCRIPTION

The EUA4992/4992A are dual bridge-connected audio power amplifiers, capable of delivering 1.25W of continuous average power to an 8Ω BTL with less than 1% distortion (THD+N) from a 5.0V power supply, and 540mW to an 8Ω BTL load from a 3.3V power supply.

The EUA4992/4992A provide high quality audio while requiring few external components and minimal power consumption. They feature a low-power shutdown mode, which is achieved by driving the $\overline{\text{SHUTDOWN}}$ pin with logic low.

The EUA4992/4992A contain circuitry to prevent from ”pop and click” noise that would otherwise occur during turn-on and turn-off transitions.
For maximum flexibility, the EUA4992/4992A provide an externally controlled gain (with resistors), as well as an externally controlled turn-on and turn-off times (with the bypass capacitor).

The EUA4992/4992A are available in a 16-pin TQFN package.

FEATURES

- Output Power at 10% THD+N, V_{DD}=5V
  -- 2.25W/CH (typ) into a 4Ω Load
  -- 1.54W/CH (typ) into a 8Ω Load
- Output Power at 1% THD+N, V_{DD}=5V
  -- 1.9W/CH (typ) into a 4Ω Load
  -- 1.25W/CH (typ) into a 8Ω Load
- Output Power at 1% THD+N, V_{DD}=3.3V
  -- 0.75W/CH (typ) into a 4Ω Load
  -- 0.54W/CH (typ) into a 8Ω Load
- Shutdown Current 0.06μA (typ)
- Supply Voltage Range 2.5V to 5.5V
- “Click and Pop” Suppression
- Thermal Shutdown Protection Circuitry
- Available in 3mmX3mm TQFN-16 (EUA4992) and 4mmX4mm TQFN-16 (EUA4992A) Packages
- RoHS compliant and 100% lead(Pb)-free

APPLICATIONS

- Cell Phones
- Portable and Desktop Computers
- Portable Audio System
- Multimedia Monitors

Typical Application Circuit

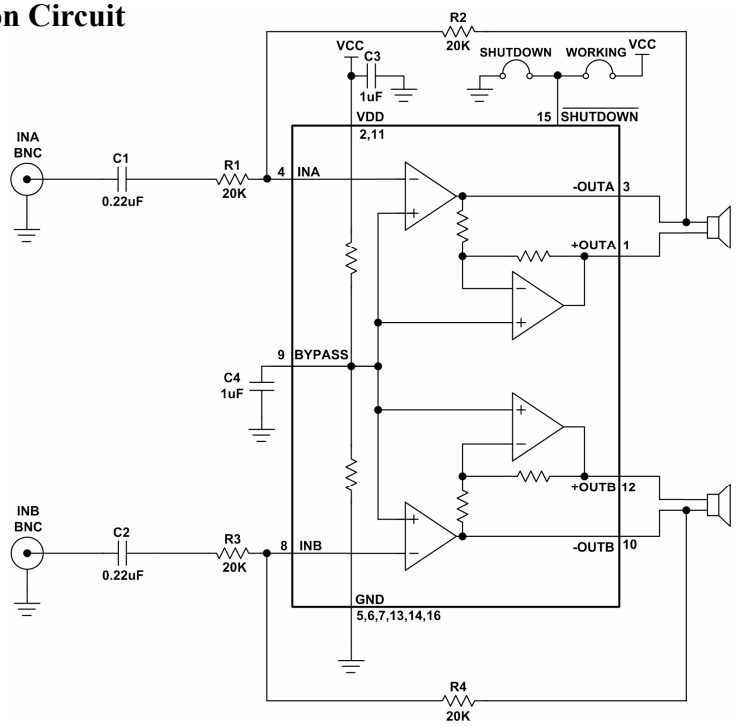
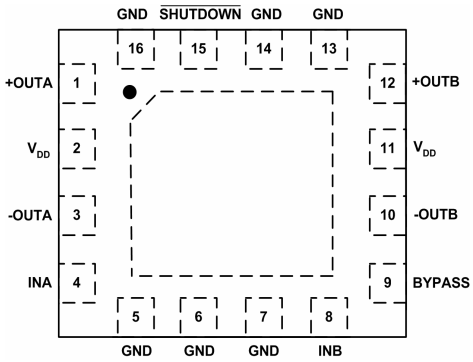


Figure 1.

Pin Configurations

Package Type	Pin Configurations
TQFN-16	

Pin Description

NAME	PIN	I/O	DESCRIPTION
INA	4	I	Left Channel Input
INB	8	I	Right Channel Input
-OUTA	3	O	Left Channel –Output
+OUTA	1	O	Left Channel +Output
-OUTB	10	O	Right Channel –Output
+OUTB	12	O	Right Channel +Output
VDD	2,11		Supply Voltage
$\overline{\text{SHUTDOWN}}$	15	I	Shutdown control, hold low for shutdown mode
BYPASS	9		Bypass capacitor which provides the common mode voltage
GND	5,6,7,13,14,16		GND

Ordering Information

Order Number	Package Type	Marking	Operating Temperature Range
EUA4992JIR1	TQFN-16	xxxxx A4992	-40 °C to +85°C
EUA4992AJIR1	TQFN-16	xxxxx 4992A	-40 °C to +85°C

EUA4992/A □ □ □ □

- Lead Free Code
  1: Lead Free 0: Lead
- Packing
  R: Tape & Reel
- Operating temperature range
  I: Industry Standard
- Package Type
  J: TQFN

Absolute Maximum Ratings

- Supply voltage ---------- 6V
- Input voltage ---------- -0.3 V to V_{DD} +0.3V
- Storage temperature rang, T_{stg} ---------- -65°C to +150°C
- Junction Temperature ---------- 150°C

Recommended Operating Conditions

	Min	Max	Unit
Supply voltage (from AC input),V_{CC}	2.5	5.5	V
Operating junction temperature range, T_J	-40	150	°C

Electrical Characteristics (5V)

The following specifications apply for V_{DD}=5V unless otherwise noted. Limits apply for T_A=+25°C.

Symbol	Parameter	Conditions	EUA4992/4992A			Unit
			Min	Typ	Max.	
V_{DD}	Supply Voltage		2.5		5.5	V
I_{DD}	Quiescent Power Supply Current	V_{IN}=0V,I_O=0A		5	8	mA
I_{SD}	Shutdown Current	GND applied to the shutdown pin		0.06	1	μA
V_{IH}	Shutdown Input Voltage High		1.1			V
V_{IL}	Shutdown Input Voltage				0.9	V
T_{WU}	Turn on time	1μF bypass cap (C4)		107		ms
V_{OS}	Output Offset Voltage	V_{IN}=0V		5	25	mV
P_O	Output Power	THD+N=1%, f=1KHz R_L=4Ω (Note 1)		1.90		W
		THD+N=1%, f=1KHz R_L=8Ω		1.25		W
		THD+N=10%, f=1KHz R_L=4Ω (Note 1)		2.25		W
		THD+N=10%, f=1KHz R_L=8Ω		1.54		W
THD+N	Total Harmonic Distortion + Noise	1KHz, Avd=2 R_L=8Ω,Po=1W		0.06		%
PSRR	Power Supply Rejection Ratio	Input grounded f=217Hz Vripple=200m Vp-p C4=1μF, R_L=8Ω		51		dB
		Input grounded f=1KHz Vripple=200m Vp-p C4=1μF, R_L=8Ω		63		
		Input unterminated f=217Hz Vripple=200m Vp-p C4=1μF, R_L=8Ω		69		
		Input unterminated f=1KHz Vripple=200m Vp-p C4=1μF, R_L=8Ω		66		
Xtalk	Channel separation	f=1KHz, C4=1μF		95		dB
V_{NO}	Output noise voltage	1KHz		11		uVrms

Note 1. The thermal performance of the QFN package when used with the exposed-DAP connected to a thermal plane is sufficient for driving 4Ω loads.

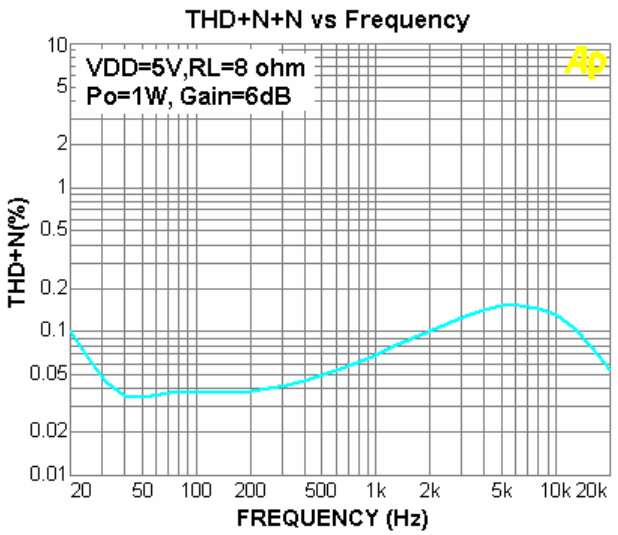
Electrical Characteristics (3.3V)

The following specifications apply for V_{DD}=3.3V unless otherwise noted. Limits apply for T_A=+25°C.

Symbol	Parameter	Conditions	EUA4992/4992A			Unit
			Min	Typ	Max.	
I_{DD}	Quiescent Power Supply Current	V_{IN}=0V,I_O=0A		3.8		mA
I_{SD}	Shutdown Current	GND applied to the shutdown pin		0.02		μA
V_{IH}	Shutdown Input Voltage High		0.9			V
V_{IL}	Shutdown Input Voltage				0.8	V
T_{WU}	Turn on time	1μF bypass cap (C4)		105		ms
V_{OS}	Output Offset Voltage	V_{IN}=0V		5		mV
P_O	Output Power	THD+N=1%, f=1KHz R_L=4Ω (Note 1)		0.75		W
		THD+N=1%, f=1KHz R_L=8Ω		0.54		W
		THD+N=10%, f=1KHz R_L=4Ω (Note 1)		0.93		W
		THD+N=10%, f=1KHz R_L=8Ω		0.64		W
THD+N	Total Harmonic Distortion + Noise	1KHz, Avd=2 R_L=8Ω,Po=0.25W		0.076		%
PSRR	Power Supply Rejection Ratio	Input grounded f=217Hz Vripple=200m Vp-p C4=1μF, R_L=8Ω		51		dB
		Input grounded f=1KHz Vripple=200m Vp-p C4=1μF, R_L=8Ω		64		
		Input unterminated f=217Hz Vripple=200m Vp-p C4=1μF, R_L=8Ω		76		
		Input unterminated f=1KHz Vripple=200m Vp-p C4=1μF, R_L=8Ω		70		
Xtalk	Channel separation	f=1KHz, C4=1μF		95		dB
V_{NO}	Output noise voltage	1KHz		11		uVrms

Note 1. The thermal performance of the QFN package when used with the exposed-DAP connected to a thermal plane is sufficient for driving 4Ω loads.

Typical Operating Characteristics



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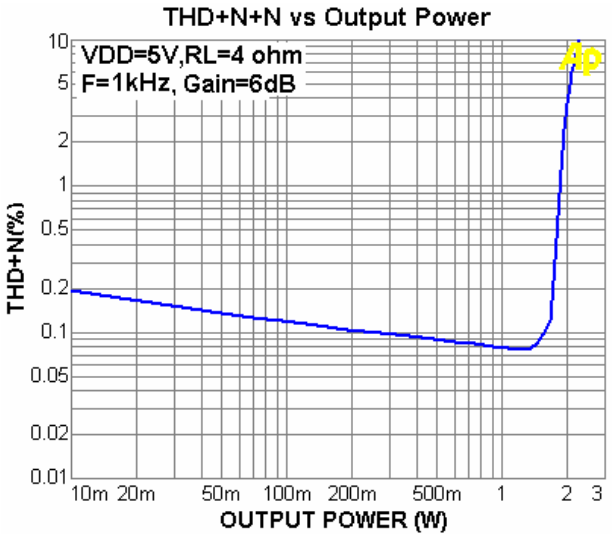

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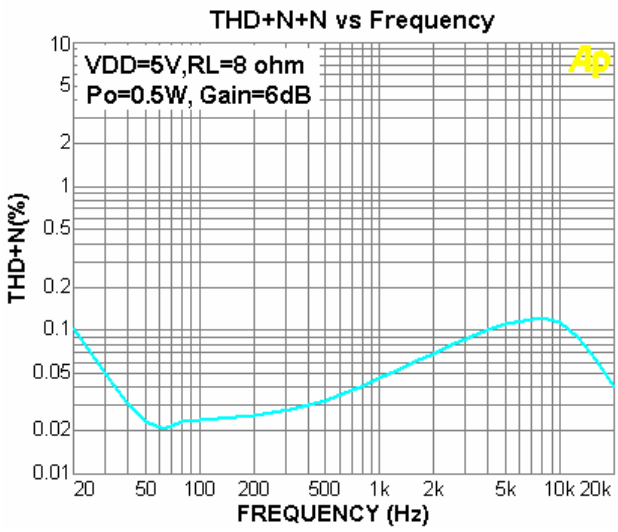

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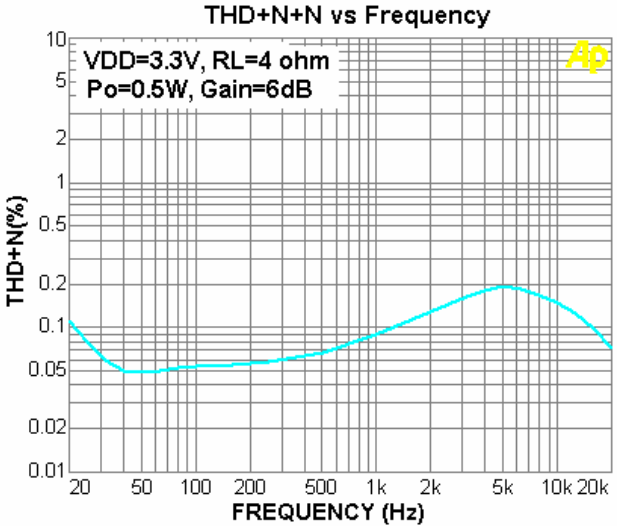

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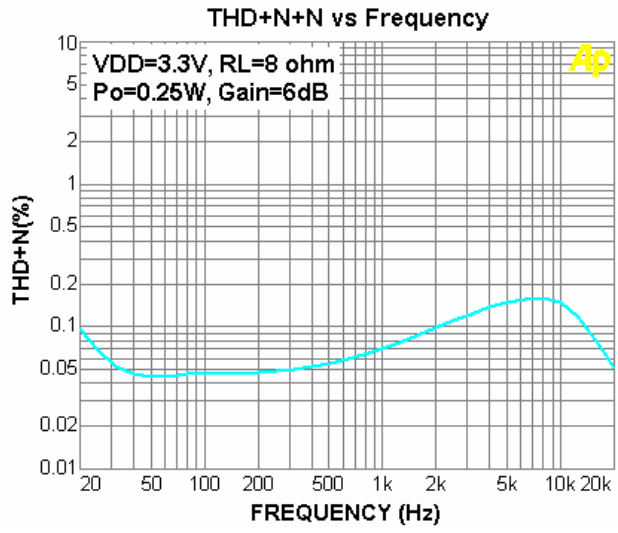

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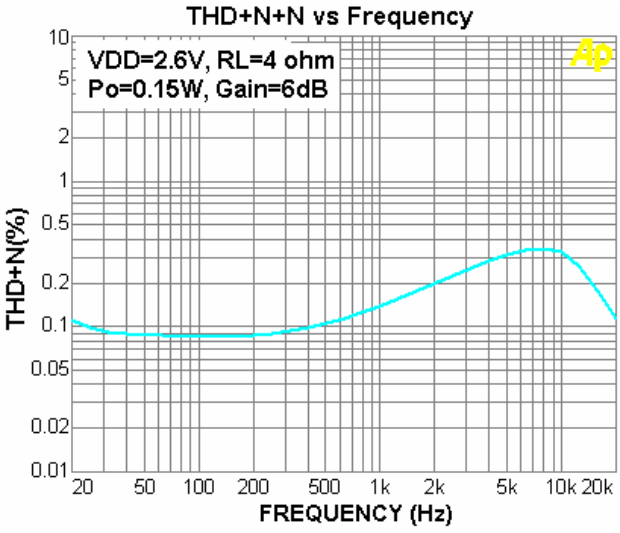

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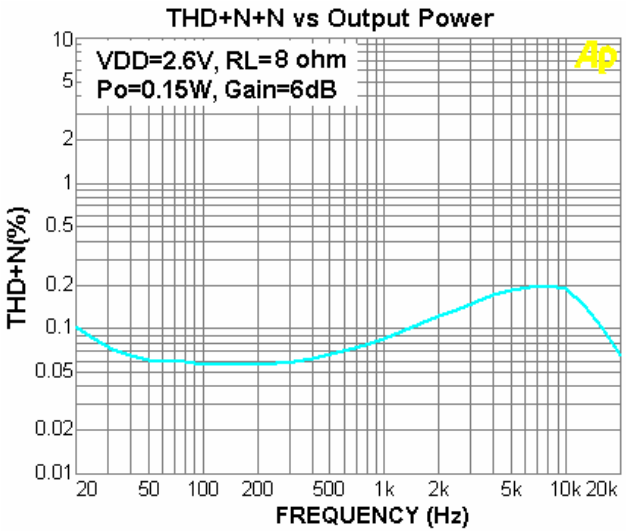

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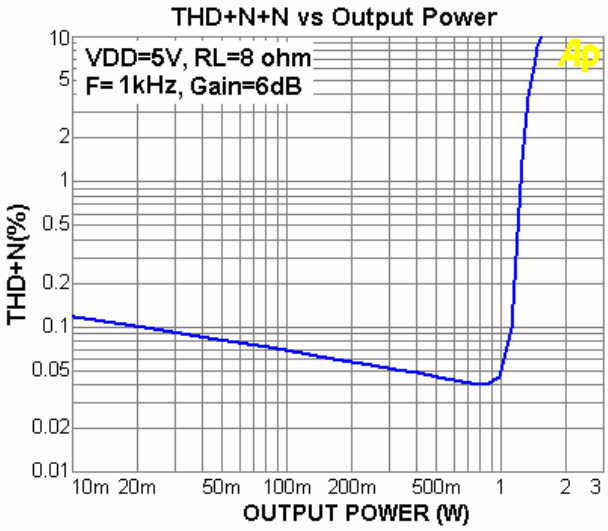

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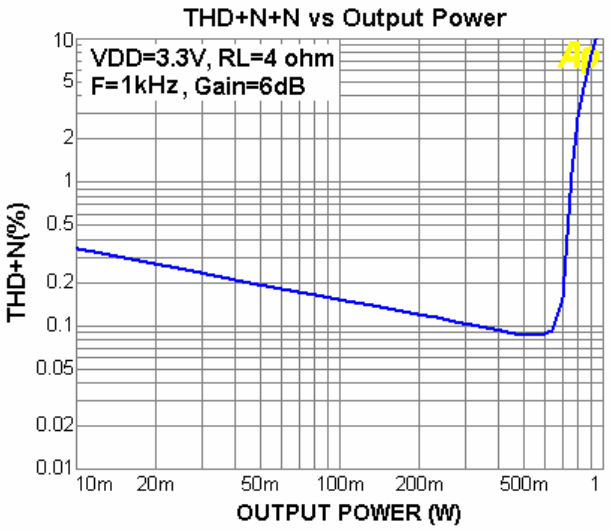

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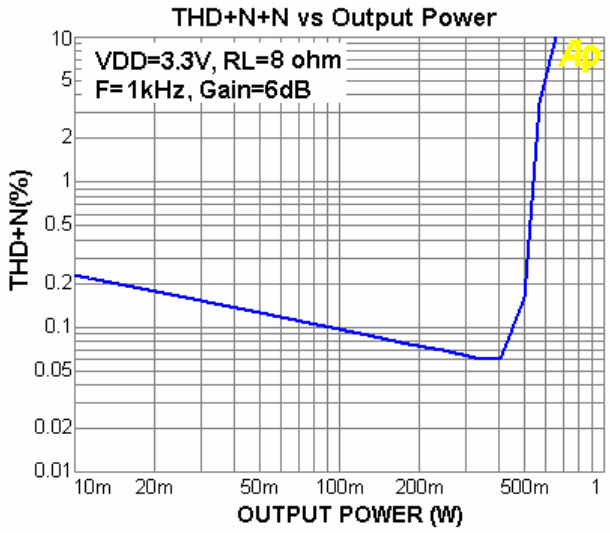

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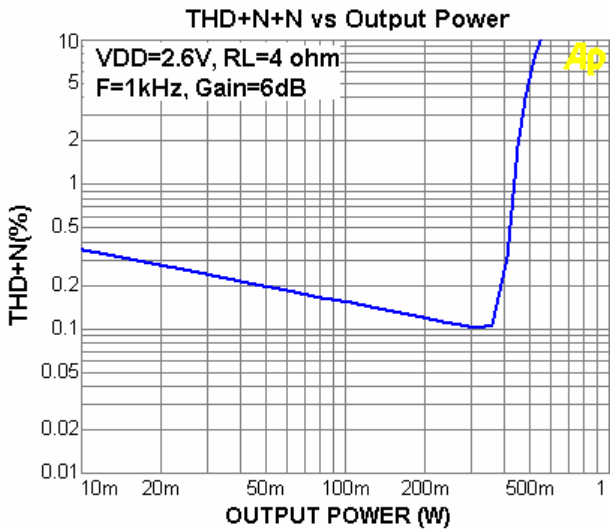

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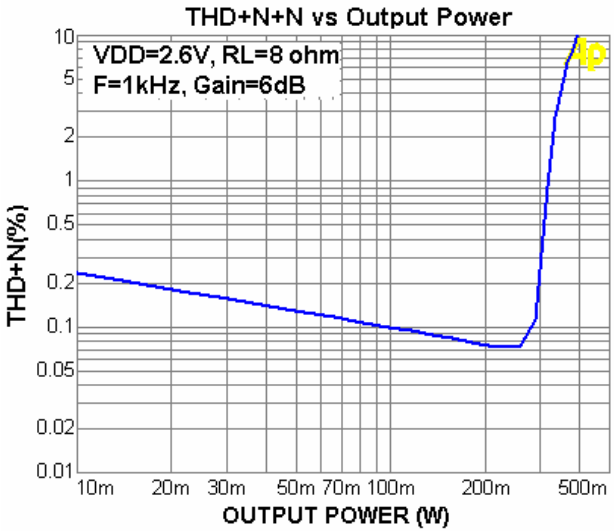

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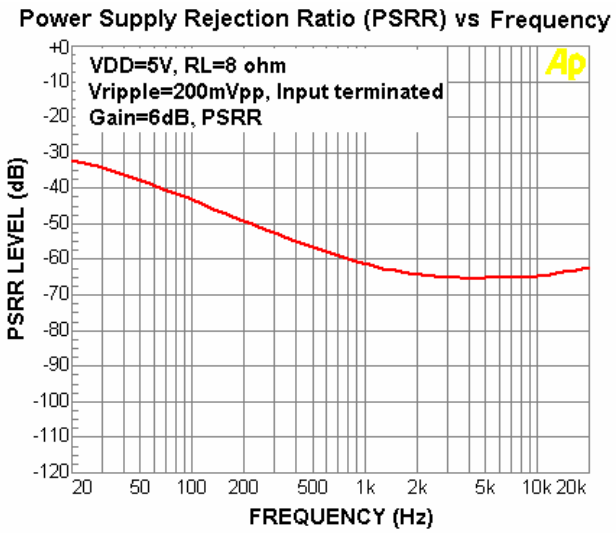

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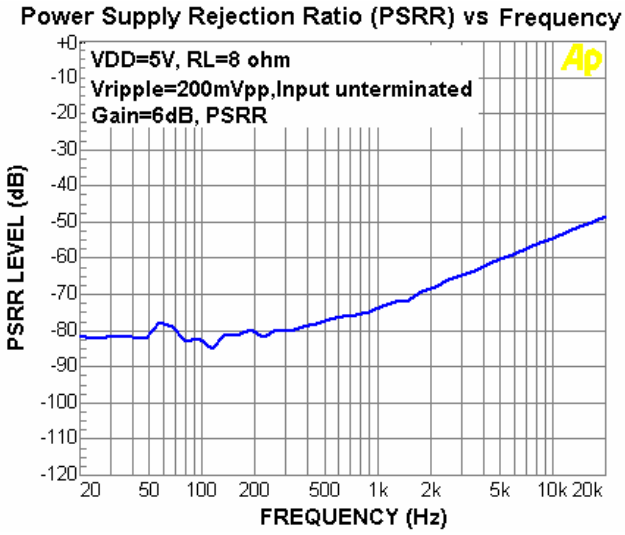

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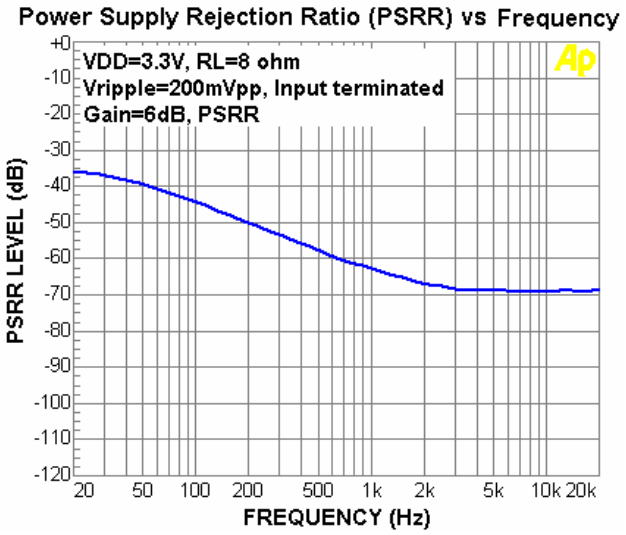

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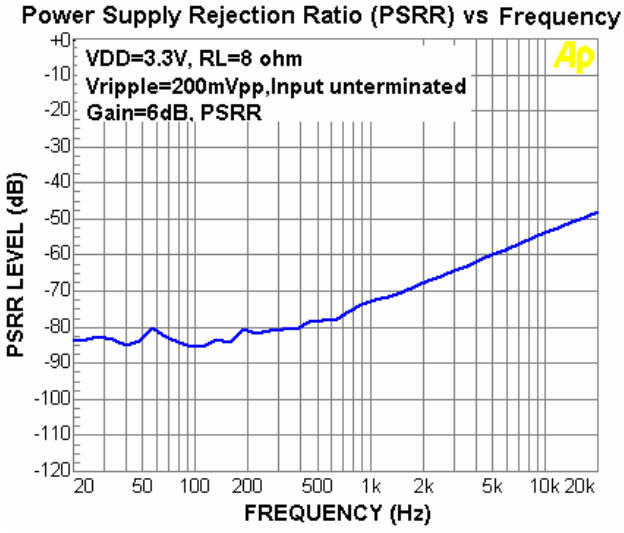

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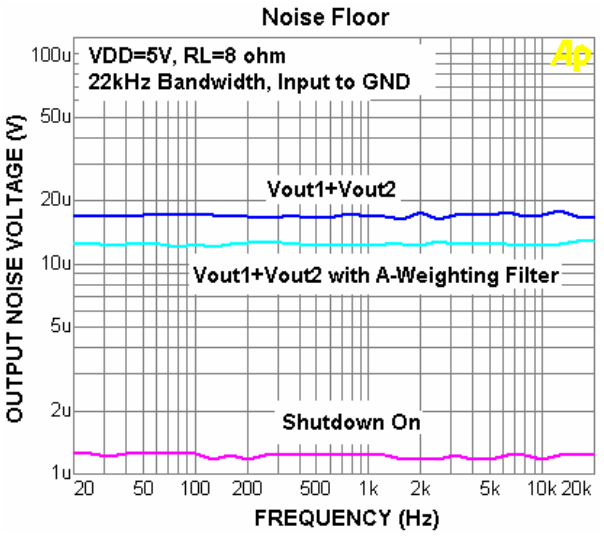

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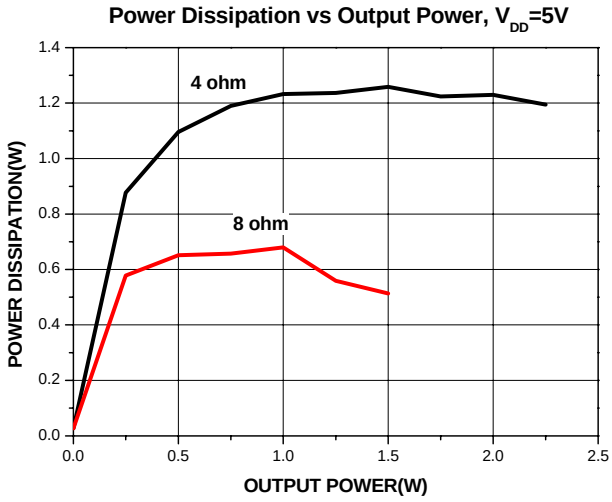

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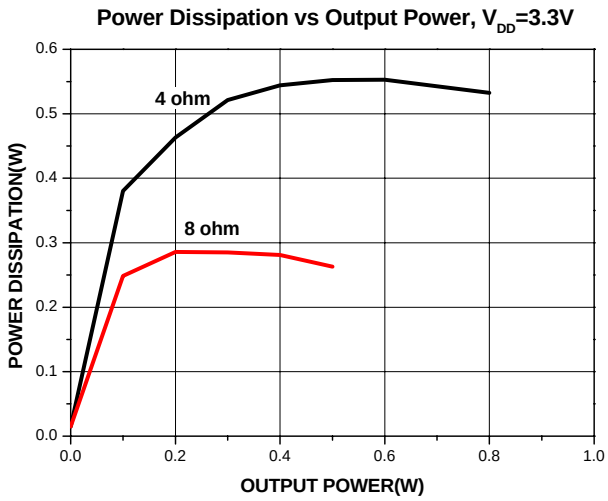

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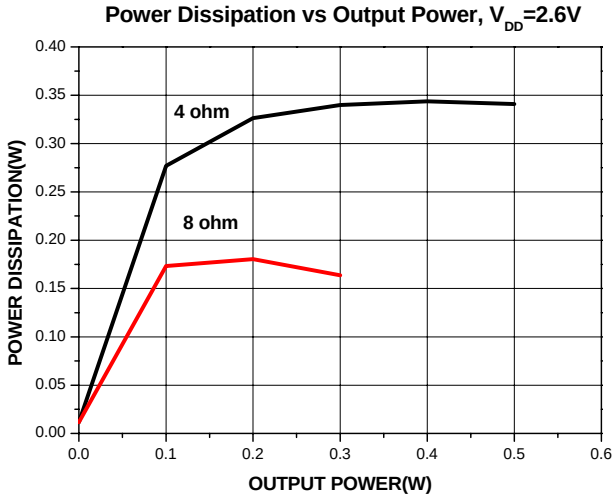

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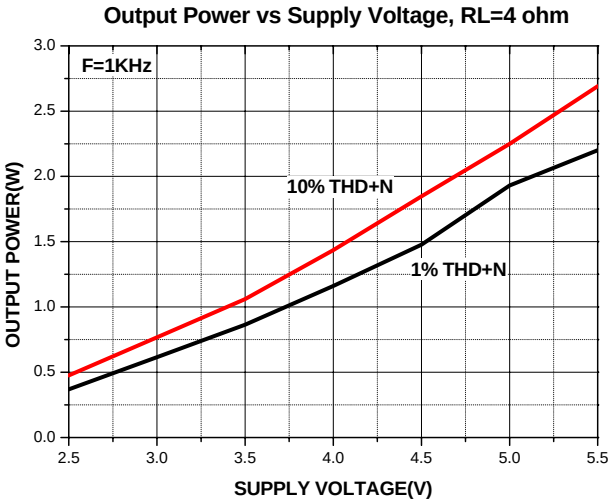

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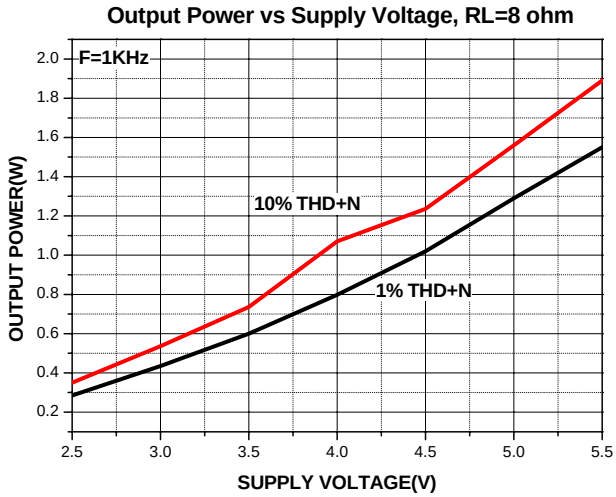

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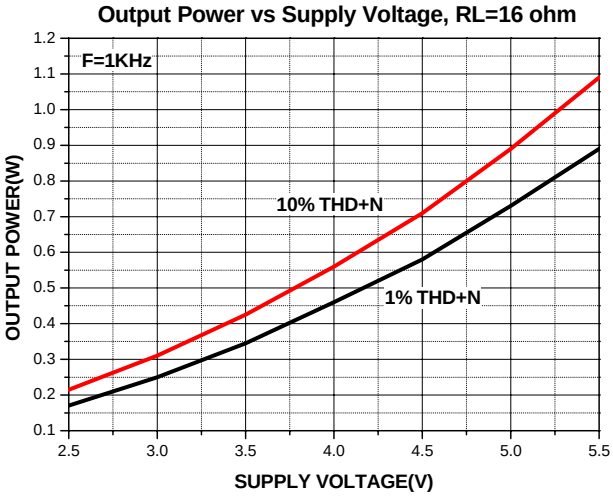

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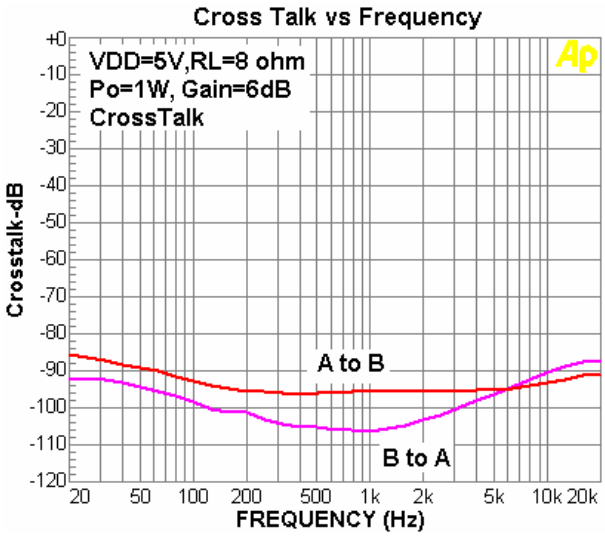

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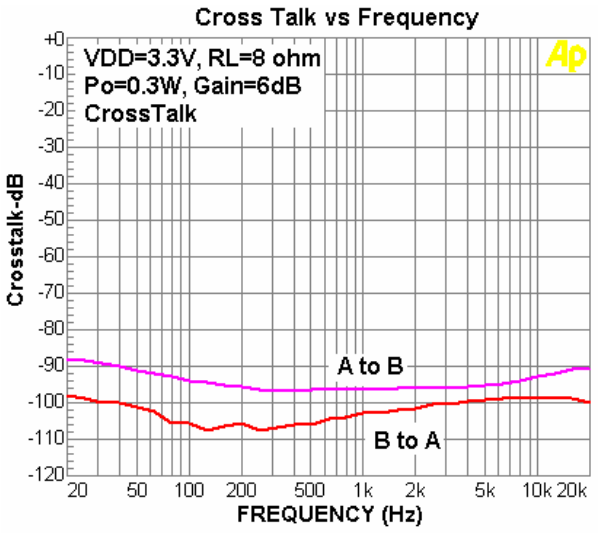


Figure26.

Application Information

Bridged Configuration Explanation

As shown in *Figure 1*, the EUA4992/4992A consists of two pairs of operational amplifiers, forming a two-channel (channel A and channel B) stereo amplifier. (Though the following discusses channel A, it applies equally to channel B.) External resistors Rf and Ri set the closed-loop gain of Amp1A, whereas two internal 20kΩ resistors set Amp2A's gain at -1. The EUA4992/4992A drives a load, such as a speaker, connected between the two amplifier outputs, -OUTA and +OUTA.

Figure 1 shows that Amp1A's output serves as Amp2A's input. This results in both amplifiers producing signals identical in magnitude, but 180° out of phase. Taking advantage of this phase difference, a load is placed between –OUTA and +OUTA and driven differentially (commonly referred to as "bridge mode"). This results in a differential gain of

$$A_{VD} = 2 \times (R_f / R_i) \qquad (1)$$

Bridge mode amplifiers are different from single-ended amplifiers that drive loads connected between a single amplifier's output and ground. For a given supply voltage, bridge mode has a distinct advantage over the single-ended configuration: its differential output doubles the voltage swing across the load. This produces four times the output power when compared to a single-ended amplifier under the same conditions. This increase in attainable output power assumes that the amplifier is not current limited or that the output signal is not clipped. To ensure minimum output signal clipping when choosing an amplifier's closed-loop gain, refer to the **Audio Power Amplifier Design** section.

Another advantage of the differential bridge output is no net DC voltage across the load. This is accomplished by biasing channel A's and channel B's outputs at half-supply. This eliminates the coupling capacitor that single supply, single ended amplifiers require. Eliminating an output coupling capacitor in a single-ended configuration forces a single-supply amplifier's half-supply bias voltage across the load. This increases internal IC power dissipation and may permanently damage loads such as speakers.

Power Supply Bypassing

As with any power amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. Applications that employ a 5V regulator typically use a 10µF in parallel with a 0.1µF filter capacitors to stabilize the regulator's output, reduce noise on the supply line, and improve the supply's transient response. However, their presence does not eliminate the need for a local 1.0µF tantalum bypass capacitance connected between the EUA4992/4992A's supply pins and ground. Do not substitute a ceramic capacitor for the tantalum. Doing so may cause oscillation in the output signal. Keep the length of leads and traces that connect capacitors between the EUA4992/4992A's power supply pin and ground as short as possible. Connecting a 1µF capacitor, C_B, between the BYPASS pin and ground improves the internal bias voltage's stability and improves the amplifier's PSRR. The PSRR improvements increase as the bypass pin capacitor value increases. Too large, however, increases turn-on time and can compromise amplifier's click and pop performance. The selection of bypass capacitor values, especially C_B, depends on desired PSRR requirements, click and pop performance (as explained in the section, **Proper Selection of External Components**), system cost, and size constraints.

Micro-Power Shutdown

The voltage applied to the SHUTDOWN pin controls the EUA4992/4992A's shutdown function. Activate micro-power shutdown by applying V_{DD} to the SHUTDOWN pin. When active, the EUA4992/4992A's micro-power shutdown feature turns off the amplifier's bias circuitry, reducing the supply current.

There are a few ways to control the micro-power shutdown. These include using a single-pole, single-throw switch, a microprocessor, or a microcontroller. When using a switch, connect an external 10kΩ pull-up resistor between the SHUTDOWN pin and V_{DD}. Connect the switch between the SHUTDOWN pin and ground. Select normal amplifier operation by closing the switch. Opening the switch connects the SHUTDOWN pin to V_{DD} through the pull-up resistor, disable micro-power shutdown. The switch and resistor guarantee that the SHUTDOWN pin will not float. This prevents unwanted state changes. In a system with a microprocessor or a microcontroller, use a digital output to apply the control voltage to the SHUTDOWN pin. Driving the SHUTDOWN pin with active circuitry eliminates the pull up resistor.

Table 1. Logic Level Truth Table for Shutdown Operation

SHUTDOWN	OPERATIONAL MODE
High	Full power, stereo BTL amplifiers
Low	Micro-power Shutdown

Selecting Proper External Components

Optimizing the EUA4992/4992A's performance requires properly selecting external components. Though the EUA4992/4992A operates well when using external components with wide tolerances, best performance is achieved by optimizing component values.

The EUA4992/4992A is unity-gain stable, giving a designer maximum design flexibility. The gain should be set to no more than a given application requires. This allows the amplifier to achieve minimum THD+N and maximum signal-to-noise ratio. These parameters are compromised as the closed-loop gain increases. However, low gain demands input signals with greater voltage swings to achieve maximum output power. Fortunately, many signal sources such as audio CODECs have outputs

of $1V_{RMS}$ ($2.83V_{P-P}$). Please refer to the **Audio Power Amplifier Design** section for more information on selecting the proper gain.

Input Capacitor Value Selection

Amplifying the lowest audio frequencies requires high value input coupling capacitor (C_i in *Figure 1*). A high value capacitor can be expensive and may compromise space efficiency in portable designs. In many cases, however, the speakers used in portable systems, whether internal or external, have little ability to reproduce signals below 150Hz. Applications using speakers with this limited frequency response reap little improvement by using large input capacitor.

Besides effecting system cost and size, C_i has an affect on the EUA4992/4992A's click and pop performance. When the supply voltage is first applied, a transient (pop) is created as the charge on the input capacitor changes from zero to a quiescent state. The magnitude of the pop is directly proportional to the input capacitor's size. Higher value capacitors need more time to reach a quiescent DC voltage (usually $V_{DD/2}$) when charged with a fixed current. The amplifier's output charges the input capacitor through the feedback resistor, R_f. Thus, pops can be minimized by selecting an input capacitor value that is no higher than necessary to meet the desired -3dB frequency.

A shown in *Figure 1*, the input resistor (R_I) and the input capacitor, C_I produce a -3dB high pass filter cutoff frequency that is found using Equation (2).

$$f_{\_3dB} = \frac{1}{2\pi R_{IN} C_I} \qquad (2)$$

As an example when using a speaker with a low frequency limit of 150Hz, C_I. The 1.0µF C_I shown in *Figure 1* allows the EUA4992/4992A to drive high efficiency, full range speaker whose response extends below 30Hz.

Bypass Capacitor Value Selection

Besides minimizing the input capacitor size, careful consideration should be paid to value of C_B, the capacitor connected to the BYPASS pin. Since C_B determines how fast the EUA4992/4992A settles to quiescent operation, its value is critical when minimizing turn-on pops. The slower the EUA4992/4992A's outputs ramp to their quiescent DC voltage (nominally 1/2 V_{DD}), the smaller the turn-on pop. Choosing CB equal to 1.0µF along with a small value of C_i (in the range of 0.1µF to 0.39µF), produces a click-less and pop-less shutdown function. As discussed above, choosing C_i no larger than necessary for the desired bandwidth helps minimize clicks and pops.

Optimizing Click and Pop Reduction Performance

The EUA4992/4992A contains circuitry to minimize turn-on and shutdown transients or "clicks and pop". For this discussion, turn-on refers to either applying the power supply voltage or when the shutdown mode is deactivated. While the power supply is ramping to its final value, the EUA4992/4992A's internal amplifiers are configured as unity gain buffers. An internal current source changes the voltage of the BYPASS pin in a controlled, linear manner. Ideally, the input and outputs track the voltage applied to the BYPASS pin. The gain of the internal amplifiers remains unity until the voltage on the bypass pin reaches 1/2 V_{DD}. As soon as the voltage on the BYPASS pin is stable, the device becomes fully operational. Although the bypass pin current cannot be modified, changing the size of CB alters the device's turn-on time and the magnitude of "clicks and pops". Increasing the value of C_B reduces the magnitude of turn-on pops. However, this presents a tradeoff: as the size of C_B increases, the turn-on time increases. There is a linear relationship between the size of C_B and the turn-on time.

In order eliminate "clicks and pops", all capacitors must be discharged before turn-on. Rapidly switching V_{DD} may not allow the capacitors to fully discharge, which may cause "clicks and pops".

Audio Power Amplifier Design

Audio Amplifier Design: Driving 1W into an 8Ω Load

The following are the desired operational parameters:

Power Output:	$1W_{RMS}$
Load Impedance:	8Ω
Input Level:	$1V_{RMS}$
Input Impedance:	20kΩ
Bandwidth:	100Hz-20 kHz ± 0.25 dB

The design begins by specifying the minimum supply voltage necessary to obtain the specified output power. One way to find the minimum supply voltage is to use the Output Power vs Supply Voltage curve in the **Typical Performance Characteristics** section. Another way, using Equation (4), is to calculate the peak output voltage necessary to achieve the desired output power for a given load impedance. To account for the amplifier's dropout voltage, two additional voltages, based on the Dropout Voltage vs Supply Voltage in the **Typical Performance Characteristics** curves, must be added to the result obtained by Equation (3). The result in Equation (4).

$$V_{opeak} = \sqrt{(2R_L P_O)} \qquad (3)$$

$$V_{DD} \geq \left(V_{OUTPEAK} + \left(V_{OD\,TOP} + V_{OD\,BOT}\right)\right) \qquad (4)$$

The Output Power vs Supply Voltage graph for an 8Ω load indicates a minimum supply voltage of 4.6V. This is easily met by the commonly used 5V supply voltage. The additional voltage creates the benefit of headroom, allowing the EUA4992/4992A to produce peak output power in excess of 1W without clipping or other audible distortion. The choice of supply voltage must also not create a situation that violates maximum power dissipation as explained above in the **Power Dissipation** section.

After satisfying the EUA4992/4992A's power dissipation requirements, the minimum differential gain is found using Equation (5).

$$A_{VD} \geq \sqrt{(P_O R_L)} / (V_{IN}) = Vorms / Vinrms \quad (5)$$

Thus, a minimum gain of 2.83 allows the EUA4992/4992A's to reach full output swing and maintain low noise and THD+N performance. For this example, let A_{VD} = 3.

The amplifier's overall gain is set using the input (R_i) and feedback (R_f) resistors. With the desired input impedance set at 20kΩ, the feedback resistor is found using Equation (6).

$$R_f / R_i = A_{VD} / 2 \quad (6)$$

The value of R_f is 30 kΩ.

The last step in this design example is setting the amplifier's -3dB frequency bandwidth. To achieve the desired ±0.25dB pass band magnitude variation limit, the low frequency response must extend to at least one-fifth the lower bandwidth limit and the high frequency response must extend to at least five times the upper bandwidth limit. The gain variation for both response limits is 0.17dB, well within the ±0.25dB desired limit. The results are an

$$f_L = 100Hz / 5 = 20Hz \quad (7)$$

and an

$$F_H = 20kHz \times 5 = 100kHz \quad (8)$$

As mentioned in the **External Components** section, R_i and C_i create a highpass filter that sets the amplifier's lower bandpass frequency limit. Find the coupling capacitor's value using Equation (9).

$$C_i \geq \frac{1}{2\pi R_i f_C} \quad (9)$$

the result is

$$1/(2\pi * 20k\Omega * 20Hz) = 0.398\mu F \quad (10)$$

Use a 0.39µF capacitor, the closest standard value. The product of the desired high frequency cutoff (100kHz in this example) and the differential gain, A_{VD}, determines the upper pass band response limit. With A_{VD} = 3 and f_H = 100kHz, the closed-loop gain bandwidth product (GBWP) is 300kHz. This is less than the EUA4992/4992A's 3.5MHz GBWP. With this margin, the amplifier can be used in designs that require more differential gain while avoiding performance-lrestricting bandwidth limitations.

Thermal Pad Considerations

The thermal pad must be connected to ground. The package with thermal pad of the EUA4992/4992A requires special attention on thermal design. If the thermal design issues are not properly addressed, the EUA4992/4992A will go into thermal shutdown when driving a heavy load.

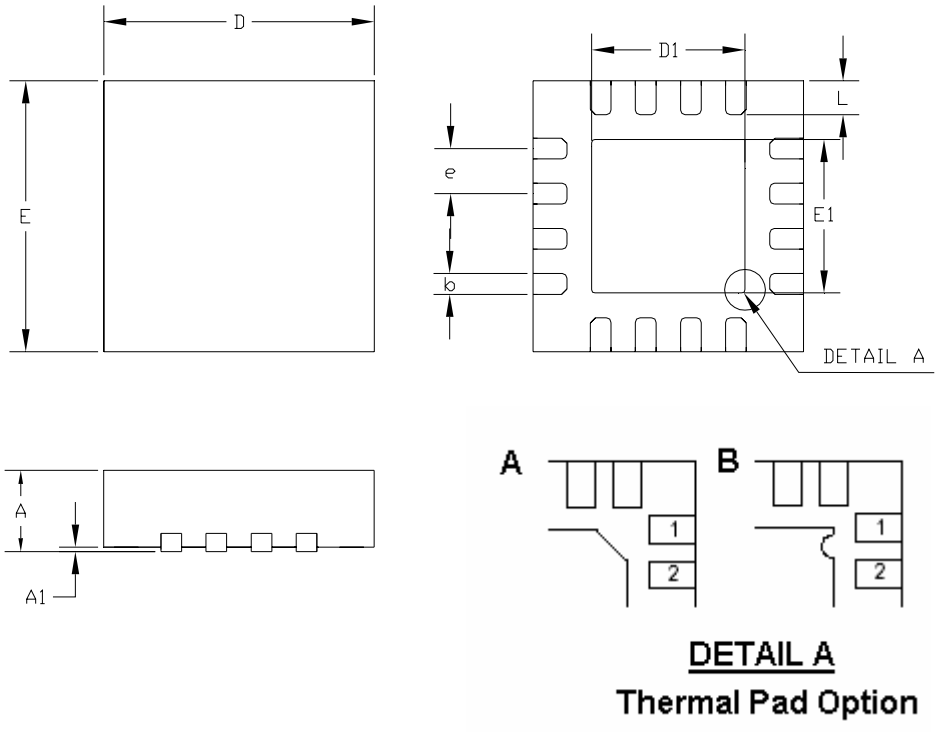
The thermal pad on the bottom of the EUA4992/4992A should be soldered down to a copper pad on the circuit board. Heat can be conducted away from the thermal pad through the copper plane to ambient. If the copper plane is not on the top surface of the circuit board, 8 to 10 vias of 13 mil or smaller in diameter should be used to thermally couple the thermal pad to the bottom plane.

For good thermal conduction, the vias must be plated through and solder filled. The copper plane used to conduct heat away from the thermal pad should be as large as practical.

If the ambient temperature is higher than 25°C,a larger copper plane or forced-air cooling will be required to keep the EUA4992/4992A junction temperature below the thermal shutdown temperature (150°C). In higher ambient temperature, higher airflow rate and/or larger copper area will be required to keep the IC out of thermal shutdown.

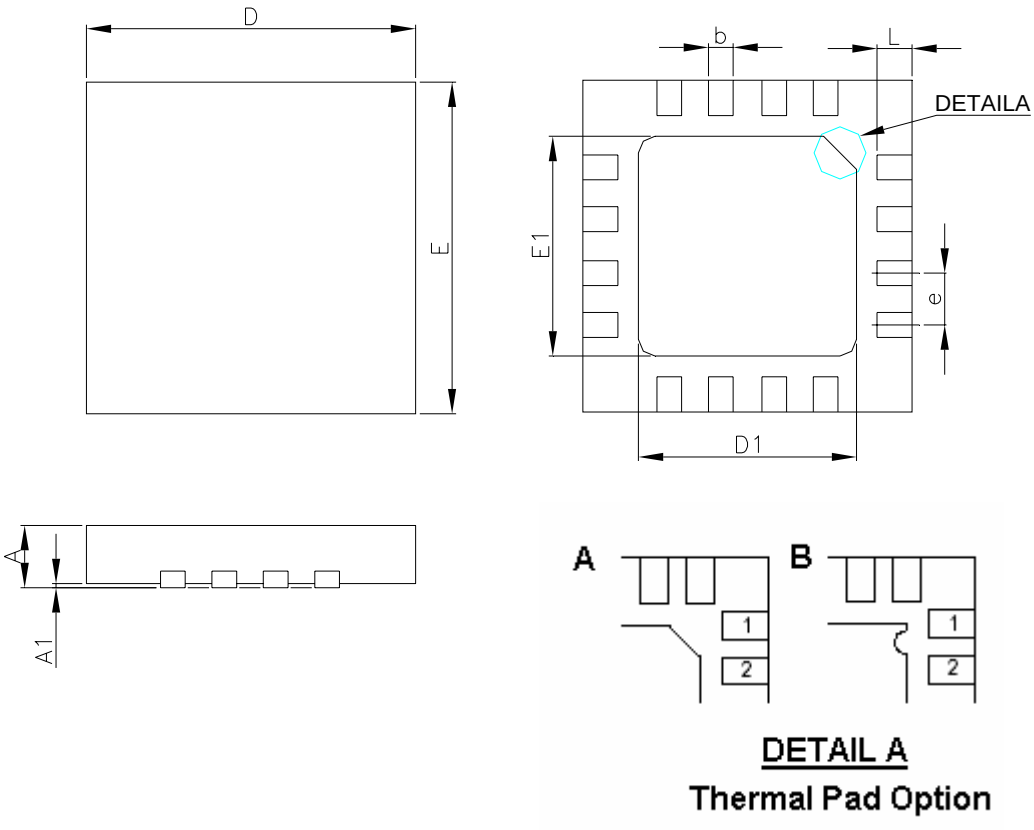
Packaging Information

TQFN-16 (3mm×3mm)



SYMBOLS	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
b	0.18	0.30	0.007	0.012
E	2.90	3.10	0.114	0.122
D	2.90	3.10	0.114	0.122
D1	1.70		0.067	
E1	1.70		0.067	
e	0.50		0.020	
L	0.30	0.50	0.012	0.020

TQFN-16 (4mm×4mm)



SYMBOLS	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
b	0.25	0.35	0.009	0.014
E	3.90	4.10	0.153	0.161
D	3.90	4.10	0.153	0.161
D1	2.50		0.098	
E1	2.50		0.098	
e	0.65		0.026	
L	0.30	0.50	0.012	0.020